The TS-V39 is an octal TigerSHARC® DSP VME card capable of nearly 12GFLOPs of performance with high-speed data I/O. Arranged in two clusters of four DSPs, each with shared memory and mezzanine I/O, the TS-V39 is ideal for radar and sonar applications, especially if low power high performance is critical. Incorporating large Xilinx Virtex-II FPGAs, the TS-V39 provides the developer with an additional processing resource which can also be used for fast data I/O and are fully customizable for FPDP, LVDS, link ports, channel-link or other digital interfaces.
ADSP-TS101 DSP
A 32-bit floating-point TigerSHARC DSP (ADSP-TS101) is capable of 1472MFLOPs (at 250MHz) with four, full-duplex 250Mbyte/sec link ports for inter-TigerSHARC DSP communications. To maximize data throughput and simplify applications development, the TigerSHARC DSP [natively] supports multiple data types and multiple calculations per cycle. The TigerSHARC DSP can achieve six 32/40-bit floating-point, twenty-four 16-bit or forty-eight 8-bit calculations per cycle. The TigerSHARC DSP can also deal with four 32-bit instructions per cycle. This together with 6Mbits of onboard memory and parallel internal databuses mean that the TigerSHARC DSP can tackle even the most demanding of applications.

Memory
In addition to the DSP on-chip SRAM, the TS-V39 has 128Mbytes of SDRAM and 4Mbytes of FLASH per cluster - accessible to both the TigerSHARC DSPs and the PCI/PMC modules and VME interface.

For embedded applications, the FLASH can be used to boot the DSP. It can also be programmed across PCI by a remote task.

FPGA Accelerated I/O
A Xilinx XC2V1000/3000 Virtex-II FPGA is available for each DSP cluster for use as a co-processor or as a high-speed digital interface.

One of the key advantages of a DSP is its ability to move large amounts data quickly and efficiently. This means that a DSP board’s I/O must be efficient so as not to starve the DSP of data. A TigerSHARC DSP based card is no exception. The TS-V39 addresses the data I/O need by providing high-speed data paths - both locally and off-board. This is achieved using both 64-bit/33MHz PCI and FPGAs connected directly to each of the DSP clusters. When used for I/O, each FPGA provides 64-connections. Since the FPGA can control the interface for one or more data streams, simple low cost I/O modules can be developed easily and quickly.

Link Ports
Link ports, a key feature of the TigerSHARC DSP, allow high-speed point-to-point communications between other TigerSHARC DSPs. This may be on the same card or between cards. The link ports are also a convenient mechanism to allow all the DSPs within the network to boot their application.

Link Port Routing
Link ports allow TigerSHARC DSP systems to easily adopt a wide range of topologies to best suit the needs of the application. The TS-V39 fully interconnects each cluster.

Peak Rates at 250MHz
16-bit performance 2 Billion MACs/sec
32-bit fixed-point performance 500 Million MACs/sec
32-bit floating-point performance 1500MFLOPS

32-bit
1k cmplx FFT (radix 2) 41µs
50-tap FIR on 1k input 110µs
Single FIR MAC 2.2ns

16-bit
256pt cmplx FFT (radix 2) 4.4µs
50-tap FIR on 1k input 29µs
Single FIR MAC 0.56ns
Single cmplx FIR MAC 2.3ns

250MHz TigerSHARC DSP Benchmark Estimates
The remaining link ports are routed to the FPDPs which are used to control the remaining connectivity. The FPDPs can route link ports between clusters or off-board via the VME P0 interface.

**VME P0 Link Ports**

Two link ports are routed to the VME P0 connector and can be used in two ways. The first, and most basic way is to fit a link port adaptor and simply hook up link port cables as required (see figure 1). An alternative is to create a PCB backplane linking up multiple boards. This is applications dependent and would normally be under taken by the systems integrator. In due course, Transtech DSP is planning to produce some off-the-shelf backplanes for standard multi-board configurations.

**Digital I/O**

As an alternative to a co-processor, the FPDPs can be used to provide a high-speed digital interface via an adapter header. Ready developed modules that Transtech supply include FPDP and LVDS. The FPDP module provides the line drivers and level-translation required and the appropriate connector through the front panel opening otherwise used by the PMC module. When using the FPDP module, the FPGA takes care of all the protocol, bus timings and data transfer. Using a similar strategy, a range of low cost modules can be developed such as LVDS for digital cameras or ADSP-2106x compatible link ports.

**Software Overview**

Software support for the TigerSHARC DSP from Transtech deals various aspects essential for effective application development:
- Low-level tools & utilities.
- Integrated Development & Debug Environments (IDEs).
- Operating Systems.

**Low-Level Tools & Utilities**

Bundled with the TS-V39 is a toolset of requisite utilities and library functions to compliment VisualDSP++ for TigerSHARC. The BSP libraries provide access to and support for Transtech DSP’s board specific functions such as interrupts, DMA driven PCI interfacing as well as runtime host communications, I/O and parallel network loaders. The toolset together with Analog Devices’ VisualDSP++ provides a minimum system configuration.

**Utilities**

The toolset includes utility tools that simplify the development of applications running on large networks of TigerSHARC DSPs.

- Network Loader
  - The network loader takes a DSP application (usually consisting of a network description file and a set of DSP executables) and loads the network from the host computer’s file system. Another related utility creates a single bootable output file that can be programmed into FLASH, allowing an application to be loaded onto the network of DSP processors from at power up.

- I/O Server
  - The I/O server runs on the host, loading the TigerSHARC DSP network and servicing I/O requests from the C runtime I/O library on the first TigerSHARC. The host server provides access to host resources such as the console and file system, using standard ANSI C calls.

- Flash Programmer
  - The TS-V39 allows up to 15 separate files to be loaded into FLASH which can then be retrieved, by name, by any TigerSHARC DSP connected to the FLASH.

**BSP Libraries**

There are a number of libraries providing support of the board hardware with both high-level routines for quick coding and also lower-level routines that allow communications to be optimized.

**C Runtime I/O Library**

A full ANSI standard library is provided for screen and file I/O from C code running on the first TigerSHARC DSP in the network. This allows a very simple way for new users to get code up and running on TigerSHARC DSP boards and provides a useful base for simple system development.

**Host Application Libraries**

Host based C++ libraries allow the writing of applications that boot a network of TigerSHARC DSPs. The libraries also support general hardware access so that the host can read/write to the DSP internal memory, Flash and any register.

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**Board Hardware Library**
To fully support the TS-V39 hardware, Transtech provides an I/O library. This includes routines to allow the TigerSHARC DSP access to other PCI cards in the system (via single cycle peek/poke cycles or high performance DMA) as well as supporting FPDP and other peripheral hardware.

**Debuggers**
A JTAG header is provided on the TS-V39 to ease debugging. This allows an Analog Devices emulator to be used with the VisualDSP++ debug tools and allows single or multi-processor debugging. Emulator hardware is also available from Transtech DSP.

**VisualDSP++**
Software development for the latest TigerSHARC DSPs is supported by the newest development tools from Analog Devices. The VisualDSP++ tool suite provides an integrated environment for developing DSP applications and also a flexible management system for DSP projects. It includes:
- Integrated Development and Debugging Environment (IDE) with VisualDSP++ Kernel (VDK) integration.
- C/C++ optimizing compiler with runtime library.
- Assembler and linker
- Simulator software with sample programs.
- Combined debugging and project management environments provide a single user interface for both development and debugging.
- Linear profiling: a debug technique that samples the target's PC register at every instruction cycle to accurately measures where instructions were executed.
- VisualDSP++ Kernel integration.

**IDE**
The integrated development, project management and debugging environment provides complete graphical control of the edit, build, and debug process.

**Development Tools**
VisualDSP++ includes a C/C++ compiler, assembler, linker, preprocessor, archiver and run-time library. VisualDSP++ supports ELF/DWARF-2 executable files. The debugger allows the developer to:
- View and debug mixed C/C++ and assembly code.
- Run TCL command-line scripts using Tool Command Language (TCL) version 8.3 to customize key debugging features.
- Use memory expressions that reference memory.
- Use breakpoints to view registers and memory.
- Statistically profile the target processor's PC while emulating.
- Linearly profile the target processor's PC while simulating.
- Graphically plot values from DSP memory.

**Run Time Libraries**
Supplied with VisualDSP++ are C and C++ run-time libraries that are collections of functions, macros, and class templates that can be called from source programs. Included in the package is a broad collection of C functions encompassing those required by the ANSI standard and additional Analog Devices-supplied functions of value for DSP programming.

**Host Operating System Support**
The host services provided by the libraries described above usually require the support of an operating system dependent device driver. Planned operating system for the TS-V39 includes:
- Windows NT4/2000 (Pentium VME)
- MVME5100/VxWorks
- VQG4/VxWorks
- SBS VG4/LynxOS
Optimized DSP Library for TigerSHARC DSP

TS-Lib is an extensive, hand-optimized assembly language library for the TigerSHARC DSP. Designed to complement Analog Devices’ run-time library (included within the VisualDSP++ tool-chain) it contains over 400 functions for signal and image processing applications.

Power Routines
Scalar, Vector, Complex Scalar Power, Complex Vector

Trigonometric Routines
Scalar & Vector Trigonometric, Scalar & Vector Hyperbolic

Vector Mathematic Routines
2-input term Vector & complex Vector, 3-input term Vector & Complex Vector, 4-input term Vector

Matrix Mathematic Routines
Matrix Vector & Scalar, Complex Matrix-Vector & Scalar

Simple Operations
Scalar, Vector, Complex Scalar, Complex Vector

Logic-Test-Sort Operations
Vector Test, Threshold, Logic, Shift, Sorting, Matrix Check

Statistic Operations
Vector Sum/Average, Vector Max/Min, Matrix Max/Min, Probability, Vector Gather/Scatter, Histogram, Integration, Interpolation

Filter Routines
Convolution, Correlation, Filtering, Windowing

Transform Routines
Conversion, Complex FFTs, Real FFTs, FFT Operator, DCT Routines, Compander, Coordinate Transform, Accumulating Spectrum

Matrix/Vector Creation & Moving Routines
Create Matrix / Vector, Complex Vector Creation, Distribution and Pseudo-Random Number Generation, Memory Move, Matrix/Vector

Other Routines
Doppler, Cholesky, Signal-Noise , Sub-matrix

TS-Lib is made available in association with EZ-DSP Ltd
## Technical Specification

**DSP**
- **Type**: 250MHz ADSP-TS101 (TigerSHARC DSP)
- **Number**: 1 or 2 clusters of 4
- **Link Port Routing**: Fully interconnected clusters, External connection via VME P0

**Memory**
- **SDRAM**: 128Mbytes per cluster
- **FLASH**: 4Mbytes per cluster (used to boot DSPs and store FPGA configuration), Programmable via PCI interface

**VME**
- **Bridge**: Tundra Universe II
- **Local PCI Device Compliance**: 64-bit PCI 2.2
- **Enhancements**: Endian swapping, DMA, interrupt support up to 528Mbytes/sec

**PMC Site**
- **Number**: 1 (single cluster version only)
- **Compliance**: 32/64-bit 33MHz, 3.3/5V signalling

**FPGA**
- **Number**: 2 (one per DSP cluster)
- **Device**: Xilinx XC2V1000 or XC2V3000 Virtex-II
- **Connectivity**: 64 user I/O signals per FPGA
- **I/O Modules**: LVDS, FPDP, Channel Link
- **Debugging**: JTAG header, 14-pin DIL header adaptor
- **Software Support**: VisualDSP++, Transtech utilities, VSPWorks, OSE, GEDAE, LynxOS, VxWorks
- **Power**: Quad DSP (15W (5V)), Octal DSP (25W (5V))
- **Environmental**:
  - **Temperature (Operating)**: 0°C to 50°C
  - **Temperature (Storage)**: -40°C to 85°C
  - **Humidity**: 0 to 95% non-condensing
  - **Vibration (Random)**: 0.02 g/Hz, 20 to 2000 Hz
  - **Shock**: 30 g peak, half sine 11 ms
  - **Conformal Coat**: No
  - **Commercial**: Yes
  - **Extended Temperature**: Yes

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